UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,762	02/21/2007	Martin Bolton	S1022.71096US00	1286

46329 7590 07/20/2010

STMicroelectronics Inc.
c/o WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
BOSTON, MA 02210-2206

EXAMINER	
KIM, HEE-YONG	

ART UNIT	PAPER NUMBER
2621	

NOTIFICATION DATE	DELIVERY MODE
07/20/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patents_eOfficeAction@WolfGreenfield.com
S1022_eOfficeAction@WolfGreenfield.com
PAIR@wolfgreenfield.com

Office Action Summary	Application No.	Applicant(s)	
	10/580,762	BOLTON ET AL.	
	Examiner	Art Unit	
	HEE-YONG KIM	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47 and 49-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-47 and 49-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/26/2006 and 2/21/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 49 is rejected under 35 U.S.C. 101 because they are directed to non-statutory subject matters.

A). Lastly, the computer program as claimed doesn't isn't properly associated with the operation. It is quite possible that the computer program may be an unrelated sub-routine or a simple commence instruction which then causes the computer to execute the operation that could be self-resident, and **not encoded on the medium**. The Examiner suggests that the computer program be more directly associated with the operation, Interim Guidelines, Annex IV (Section b). Corrections to the claims, and supporting specification are required.

Computer program per se is not statutory. One requirement is to store into non-transitory computer readable medium. The examiner recommends rewriting claim to begin as "A non-transitory computer readable medium ...."

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 6 and 36** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 6 and 36 recite "and/or" which is indefinite. For the prosecution of the application, the examiner interprets as "or".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-11, 14-23, 27, 31-41, 43-45, 49, and 51** are rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto (US 5,646,688).

Regarding **claim 1**, Hashimoto discloses Video Decoder Architecture Using Separate Semiconductor Substrates. Specifically Hashimoto discloses A video decoding circuit (video data decoding system, Fig.1) comprising:

a first video data processor (first semiconductor substrate 12, Fig.1) ; a second video data processor (second semiconductor substrate 14, Fig.1); and a connection connecting (buses internal, col.2, line 40) said first video data processor and said second data processor; wherein said first video data processor is arranged to receive a first signal comprising encoded video data (encoded input, col.2, line 44), process said first signal to provide a second signal and output said second signal (motion vector and IDCT output, Fig.1), said first video data processor being

arranged to process said first signal dependent on at least part (decoding motion vectors by parser 20 and dequantizing the quantized DCT coefficients by 22 and 24, Fig.1) of said received first signal, and

said second video data processor comprising a predictor constructor (Motion compensation unit 26a, Fig.1), said second video data processor is arranged to receive at least a part of said second signal (motion vector and IDCT output, Fig.1), process said at least a part of said second signal (motion vector and IDCT output, Fig.1) to provide a third signal (I-picture, B-picture, and P-picture, Fig.1), and output said third signal (output, fig.1), said second and third signals comprising a decoded video image stream wherein a part of said second signal comprises a picture level parameter word (it was well know in the art that MPEG bitstream has picture level information such as picture type (I,P,B type) and display order in the picture header and Parser 20 at Fig.1 decode this information into second signal) which comprises coding standard information (MPEG syntax, col.2, line 24), said coding standard information defining variations (It was well known in the art that MPEG syntax includes Sequence level, Picture level, slice level, macroblock level information) in the type of data, and

said second video data processor is arranged to process said at least part of said second signal (motion vector and IDCT output, Fig.1) dependent on the format of the data received (it was well known in the art that macroblock type (intra or inter) dictates whether motion compensation is needed).

Regarding **Claim 2**, Hashimoto discloses everything claimed as applied above (see claim 1). In addition, Hashimoto discloses wherein said first video data processor

is arranged to variable length decode (decode Huffman-encoding, col.3, line 15-16) said received first signal to produce a decoded first signal.

Regarding **Claim 3**, Hashimoto discloses everything claimed as applied above (see claim 2). In addition, Hashimoto discloses wherein said first video data processor

is arranged to separate said first signal data into at least a first part and a second part,

wherein said first part comprises at least one of:

pixel data (Input to Dequantization (22, Fig.1) when macroblock is intra type);

residual data (Input to Dequantization (22, Fig.1) when macroblock is inter type), and

wherein said second part comprises motion vector data (motion vector, Fig.1).

Regarding **Claim 4**, Hashimoto discloses everything claimed as applied above (see claim 3). In addition, Hashimoto discloses wherein said first video data processor

is arranged to inverse quantize (Dequantization 22, Fig.1) said first part of said first signal.

Regarding **Claim 5**, Hashimoto discloses everything claimed as applied above (see claim 3). In addition, Hashimoto discloses wherein said first video data processor is arranged to spatial domain transform (IDCT 24, Fig.1) said first part of said first signal.

Regarding **Claim 6**, Hashimoto discloses everything claimed as applied above (see claim 4). In addition, Hashimoto discloses wherein said first video data processor is arranged to combine said spatial domain transformed (IDCT 24, Fig.1) and/or inverse quantized first part of said first signal (Dequantization 22, Fig.1) with said second part (motion vector, Fig.1) of said first signal.

Regarding **Claim 7**, Hashimoto discloses everything claimed as applied above (see claim 1). In addition, Hashimoto discloses wherein said second video data

processor is arranged (calculate motion compensated frame, col.4, line 38-40) to interpolate (averaging values for neighboring pixels, col.4, line 45-46) at least a first part (IDCT(24,Fig.1) output, which is an image pixel data) of said second signal..

Regarding **Claim 8**, Hashimoto discloses everything claimed as applied above (see claim 7). In addition, Hashimoto discloses wherein said second video data processor is arranged (calculate motion compensated frame, col.4, line 38-40) to interpolate at least a first part (IDCT(24,Fig.1) output, which is an image pixel data) of said second signal using one of horizontal and vertical interpolation (averaging values for neighboring pixels, col.4, line 45-46).

Regarding **Claim 9**, Hashimoto discloses everything claimed as applied above (see claim 8). In addition, Hashimoto discloses further comprising a memory (input buffer 30 and 36, Fig.1), said second video data processor being arranged to store said interpolated part of said second signal in said memory.

Regarding **Claim 10**, Hashimoto discloses everything claimed as applied above (see claim 8). In addition, Hashimoto discloses wherein said second video data processor is arranged to interpolate said stored interpolated first part of said second signal using the other one of horizontal and vertical interpolation (it was well known in the art that when half pixel position is at the center of four surrounding pixels, it is interpolated in one direction (horizontally or vertically) first (horizontally for top and bottom, or vertically for left and right of half pixel position) and then interpolate (average) in the other direction).

Regarding **Claim 11**, Hashimoto discloses everything claimed as applied above (see claim 7). In addition, Hashimoto discloses wherein said second video data processor is arranged

to combine (summation unit (42, fig.1) sum, col.4, line 39-43) said interpolated part (compensated frame, col.4, line 39-43) of said second signal and a further part (differential signal (IDCT output, Fig.1), col.4, line 39-43) of said second signal, wherein said interpolated part of said second signal comprises an estimated macro block (prediction, col.1, line 40-42), and said further part of said second signal comprises residual error data (differential data, col.1, line 40-42).

Regarding **Claim 14**, Hashimoto discloses everything claimed as applied above (see claim 1). In addition, Hashimoto discloses wherein said connection comprises a bus (buses internal, col.2, line 40) connecting said first and second video data processors.

Regarding **Claim 15**, Hashimoto discloses everything claimed as applied above (see claim 14). In addition, Hashimoto discloses further comprising a memory device (Input Buffer 28, Fig.1), said memory device being connected to said bus (buses internal, col.2, line 40).

Regarding **Claim 16**, Hashimoto discloses everything claimed as applied above (see claim 15). In addition, Hashimoto discloses wherein said first video data processor has an output (IDCT (24, Fig.1) output) for outputting said second signal to said memory device (Input Buffer 28, Fig.1) via said bus.

Regarding **Claim 17**, Hashimoto discloses everything claimed as applied above (see claim 16). In addition, Hashimoto discloses wherein said second video data processor has an input (input to Input buffer 28, fig.1) for receiving said parts of said second signal from said memory device via said bus.

Regarding **Claim 18**, Hashimoto discloses everything claimed as applied above (see claim 1). In addition, Hashimoto discloses wherein said connection comprises a data

interconnect (8-bit buses, col.5, line 54-58) said data interconnect directly (As shown in Fig.1, the buses are dedicated between two processors, therefore they are interconnect directly) connecting said first video data processor and said second video data processor.

Regarding **Claim 19**, Hashimoto discloses everything claimed as applied above (see claim 18). In addition, Hashimoto discloses wherein said first video data processor has an output for outputting said second signal (8-bit bus for motion vectors and 8-bit bus to provide for input to input buffer 28, col.5, line 54-58) to said data interconnect.

Regarding **Claim 20**, Hashimoto discloses everything claimed as applied above (see claim 18). In addition, Hashimoto discloses wherein said second video data processor has an input (input to input buffer 28) for receiving said parts of said second signal from said data interconnect.

Regarding **Claim 21**, Hashimoto discloses everything claimed as applied above (see claim 20). In addition, Hashimoto discloses wherein said connection comprises a bus (8-bit bus for motion vectors and 8-bit bus to provide for input to input buffer 28, col.5, line 54-58) connecting said first and second video data processors and further comprising a memory device (input to input buffer 28, col.5, line 54-58), said memory device being connected to said bus wherein said second video data processor receives part of said parts of said second signal from said data interconnect (bus is also data interconnect) and part of said parts of said second signal from said bus.

Regarding **Claim 22**, Hashimoto discloses everything claimed as applied above (see claim 1). In addition, Hashimoto discloses wherein said first signal is at least one of a MPEG2 encoded video stream (MPEG, col.4, line 6); a H. 263 encoded video stream; a RealVideo9

encoded video stream; a Windows media player encoded video stream; a H. 264 encoded video stream.

Regarding **Claim 23**, Hashimoto discloses everything claimed as applied above (see claim 1). In addition, Hashimoto discloses wherein said

second signal comprises at least one of: buffer base address word; picture level parameter header word; macro-block header word; slice parameter word; motion vector horizontal luma word (motion vector, Fig.1, and it was well known that motion vector consist of a luma horizontal and vertical components); motion vector vertical luma word (motion vector, Fig.1, and it was well known that motion vector consist of a luma horizontal and vertical components); motion vector horizontal chroma word ; motion vector vertical chroma word; pixel data reference word and pixel data residual word (IDCT output, Fig.1).

Regarding **Claim 27**, Hashimoto discloses everything claimed as applied above (see claim 1). In addition, Hashimoto discloses An integrated circuit (first and second semiconductor substrates 12 and 14, Fig.1) comprising a circuit.

Regarding **Claim 31**, the claim is a method claim corresponding to the apparatus claim 1. Therefore, it is rejected for the same reason as claim 1.

Regarding **Claim 32**, the claim is a method claim corresponding to the apparatus claim 2. Therefore, it is rejected for the same reason as claim 2.

Regarding **Claim 33**, the claim is a method claim corresponding to the apparatus claim 3. Therefore, it is rejected for the same reason as claim 3.

Regarding **Claim 34**, the claim is a method claim corresponding to the apparatus claim 4. Therefore, it is rejected for the same reason as claim 4.

Regarding **Claim 35**, the claim is a method claim corresponding to the apparatus claim 5. Therefore, it is rejected for the same reason as claim 5.

Regarding **Claim 36**, the claim is a method claim corresponding to the apparatus claim 6. Therefore, it is rejected for the same reason as claim 6.

Regarding **Claim 37**, the claim is a method claim corresponding to the apparatus claim 7. Therefore, it is rejected for the same reason as claim 7.

Regarding **Claim 38**, the claim is a method claim corresponding to the apparatus claim 8. Therefore, it is rejected for the same reason as claim 8.

Regarding **Claim 39**, the claim is a method claim corresponding to the apparatus claim 9. Therefore, it is rejected for the same reason as claim 9.

Regarding **Claim 40**, the claim is a method claim corresponding to the apparatus claim 10. Therefore, it is rejected for the same reason as claim 10.

Regarding **Claim 41**, the claim is a method claim corresponding to the apparatus claim 11. Therefore, it is rejected for the same reason as claim 11.

Regarding **Claim 43**, the claim is a method claim corresponding to the apparatus claim 16. Therefore, it is rejected for the same reason as claim 16.

Regarding **Claim 44**, the claim is a method claim corresponding to the apparatus claim 18. Therefore, it is rejected for the same reason as claim 18.

Regarding **Claim 45**, the claim is a method claim corresponding to the apparatus claim 21. Therefore, it is rejected for the same reason as claim 21.

Regarding **Claim 49**, the claim is a computer readable medium claim corresponding to the apparatus claim 1. Therefore, it is rejected for the same reason as claim 1.

Regarding **Claim 51**, Hashimoto discloses everything claimed as applied above (see claim 1). In addition, Hashimoto discloses An MPEG decoder (decoding a MPEG data stream, col.4, line 4-6) comprising a circuit as claimed in claim 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 12-13, and 42** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto in view of Gomila (US 2003/0,206,664) (hereafter referenced as Gomila).

Regarding **claim 12**, Hashimoto discloses everything clamed as applied above (see claim 11). However Hashimoto fails to disclose wherein said second video data processor is arranged to filter at least one of said at least one part of said second signal and said third signal.

In the analogous field of endeavor, Gomila discloses Deblocking Filter Conditioned on Pixel Brightness. Specifically Gomila discloses deblocking *filtering* of reconstructed signal (*said third signal)* (Deblocking Filter 240, Fig.2), in order to reduce blockiness artifact (paragraph 4).

Therefore, given this teaching, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify Hashimoto by specially incorporating deblocking filter in the second video data processor, in order to reduce blockiness artifact. The Hashimoto video data processing architecture, incorporating the Gomila deblocking filter in the second semiconductor substrate, has all the features of claim 12.

Regarding **claim 13**, The Hashimoto video data processing architecture, incorporating the Gomila deblocking filter in the second semiconductor substrate, as applied to claim 12, discloses wherein said filter comprises at least one of a de-ringing filter and a deblocking filter *)* (Gomila: Deblocking Filter 240, Fig.2).

Regarding **Claim 42**, the claim is a method claim corresponding to the apparatus claim 13. Therefore, it is rejected for the same reason as claim 13.

8. **Claims 24-26, and 46-47** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto in view of Wu (US 6,415,345) (hereafter referenced as Wu).

Regarding **claim 24**, Hashimoto discloses everything clamed as applied above (see claim 11). However Hashimoto fails to disclose wherein said first video data processor comprises a data packer.

In the analogous field of endeavor, Wu discloses Bus Mastering Interface Control System for Transferring Multistream Data Over a Host Bus. Specifically Wu discloses data packer (122 at Fig.1) with a host bus (108, Fig.1), in order to pack valid data in fixed sized unit to form a packet (col.3, line 47-50).

Therefore, given this teaching, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify Hashimoto by specifically incorporating data packer in the first video data processor with a host bus between first and second video data processors, in order to pack valid data in fixed sized unit to form a packet. The Hashimoto video data processing architecture, incorporating the Wu data packer in the first video data processor with a host bus, has all the features of claim 24.

Regarding **claim 25**, the claimed invention is same as claim 24 except that data packer is in the second video processor instead of first. Two claimed inventions are equivalent and one is an obvious variation of the other. And therefore, it is obvious over Hashimoto in view of Wu.

Regarding **claim 26**, the Hashimoto video data processing architecture, incorporating the Wu data packer in the first video data processor with a host bus, as applied to claim 24, discloses wherein said data packer comprises: an input (Wu: input to bus mater FIFO controller 124, Fig.1), said input being arranged to receive said second signal (Hashimoto: motion vector and IDCT output, Fig.1), said second signal comprising data words (Hashimoto: motion vectors and IDCT output); means for ordering said data words (Wu: pack valid data in fixed sized unit to form a packet, col.3, line 47-50);

and an output (Wu: output to host bus 108, Fig.1), said output being arranged to transmit data packets comprising ordered data words.

Regarding **Claim 46**, the claim is a method claim corresponding to the apparatus claim 24. Therefore, it is rejected for the same reason as claim 24.

Regarding **Claim 47**, the claim is a method claim corresponding to the apparatus claim 26. Therefore, it is rejected for the same reason as claim 26.

9. **Claims 28-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto in view of Trivedi (US 6,573,846) (hereafter referenced as Trivedi).

Regarding **claim 28**, Hashimoto discloses everything clamed as applied above (see claim 1). However Hashimoto fails to disclose wherein said first video data processor comprises a very long instruction word processor.

In the analogous field of endeavor, Trivedi discloses Method and Apparatus for Variable Length Decoding and Encoding of Video Stream. Specifically Wu discloses wherein said first video data processor comprises a very long instruction word processor (Media Processor using very long instruction word (VLIW), Fig.5A) for decoding MPEG bitstream such VLD (Variable length decoding) (8303, Fig.63) and IDCT (8304 at Fig.63), in order to issue the instructions to different functional units in the media processor in the same clock cycle (col.2, line 17-24).

Therefore, given this teaching, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify Hashimoto by specifically providing VLIW processing to the first video processor, in order to issue the instructions to different functional units in the media processor in the same clock cycle. The Hashimoto video data processing architecture, incorporating the Trivedi VLIW processing architecture to the first video processor, has all the features of claim 28.

Regarding **claim 29**, the Hashimoto video data processing architecture, incorporating the Trivedi VLIW processing architecture to the first video processor, as applied to claim 28, discloses wherein said very long instruction word processor is adapted to process said first signal further (programmed by instructions) dependent on a set of instructions stored in a memory (cache 1504 and host memory 1506, Fig.5A) .

10. **Claims 30, 50, and 52** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto.

Regarding **claim 30**, Hashimoto discloses everything clamed as applied above (see claim 1). However Hashimoto fails to disclose wherein said second video data processor comprises a programmable processor.

However, it was well known in the art that the functions of second video processor is performed by programmable processor such as DSP (digital signal processor), in order to have a flexibility of programming.

Therefore, given this teaching, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify Hashimoto by specially providing DSP to the second video processor, in order to have a flexibility of programming. The Hashimoto video data processing architecture, incorporating DSP to the second video processor, has all the features of claim 30.

Regarding **claim 50**, Hashimoto discloses everything clamed as applied above (see claim 1). However Hashimoto fails to disclose A Digital Versatile Disc device comprising a circuit as claimed in claim 1.

However, it was well known in the art that DVD is storing MPEG encoded bitstream. Therefore, it requires MPEG decoder and the Hashimoto MPEG video decoder architecture is obvious to try to use, in order to play DVD movie.

Regarding **claim 52**, Hashimoto discloses everything clamed as applied above (see claim 1). However Hashimoto fails to disclose A Digital Video Broadcasting device comprising a circuit as claimed in claim 1.

However, it was well known in the art that DVB broadcasting is using MPEG standard bitstream. Therefore, DVB receiver requires MPEG decoder and the Hashimoto MPEG video

decoder architecture is obvious to try to use, in order to play the video transmitted by DVB broadcasting.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HEE-YONG KIM whose telephone number is (571)270-3669. The examiner can normally be reached on Monday-Thursday, 8:00am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha Banks-Harold can be reached on 571-272-7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

.

/HEE-YONG KIM/
Examiner, Art Unit 4192

/Andy S. Rao/
Primary Examiner, Art Unit 2621
July 15, 2010